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Origin of Hysteresis in Zinc Oxide Based Metal Oxide Semiconductor Films

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Abstract

Zinc oxide is a unique material that exhibits semiconducting and piezoelectric dual properties. Interfacing of oxide and semiconductor materials provides a means of coupling unique properties associated with oxide materials to high performance semiconductor devices. To function at low biases to minimize power consumption, such devices must also contain a high-mobility semiconductor and/or a high-capacitance gate oxide. In this work we ovserve the crystal quality and composition of the deposited films with atomic force microscopy (AFM), scanning electron microscopy (SEM), Rutherford backscattering (RBS) and X-ray photoelectron spectroscopy (XPS) and electrical properties of SiO_2/ZnO heterostructure, where SiO_2 is used as oxide. Metal–Oxide–Semiconductor structures demonstrate hysteresis characteristic. The metal–SiO_2–ZnO capacitor structures demonstrate a characteristic metal–insulator–semiconductor capacitance–voltage (C-V) behaviour with a hysteretic memory window of approximately 0.12 V. The appearance of a broad hysteresis and the significant shift in the flatband voltage indicate the presence of a large number of trapped charges at the interfaces.

Keywords:

Zinc Oxide;
Metal Oxide Semiconductor;
XPS;
RBS;
SEM.

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1. Introduction

Information Technology, which has improved the quality of our daily life, has become one of the most important technologies. Therefore, the performances of electronic devices need to be improved very rapidly. In 1965, Gordon Moore, co-founder of Intel, predicted that the number of components (transistors) per integrated circuit, or in other words processing capacity and speed, will double every 12-18 months. Silicon dioxide (SiO_2) has been as the primary gate dielectric material in field-effect devices since 1957 due to good interface, low gate leakage currents and excellent thermal (structural) stability at Si process temperatures. Since then, SiO_2 has been successfully scaled down for the device's high performance with much effort towards current technologies of 0.13~0.18 μm [1]. Thermally grown rapid thermal oxynitrides with equivalent oxide thickness (EOT) of 18~25 Å has been introduced in the manufacturing area for the replacement of SiO_2. The technology for beyond 0.1μm requires further thickness scaling of SiO_2 or oxynitride and is approaching their scaling limits. However, it has been realized that use of gate oxide, scaled below 10Å, will be limited by breakdown, plasma damage, carrier mobility degradation, or poly depletion effect [2]. Because SiO_2 of 10Å physical thickness would be only three monolayers thick, gate oxide scaling is limited due to direct tunneling currents, since the tunneling current increases exponentially with decreasing physical thickness of SiO_2. Pure ZnO is a nonstochiometric n-type semiconductor [3]. ZnO crystallites into a wurtzite structure [4], i.e. a complete hcp-lattice with oxygen atoms are inserted into the zinc hcp-lattice. The need for a stable semiconductor with good electronic properties, compatible with low temperature silicon substrates, motivated us to investigate ZnO as a semiconductor for MOSFET applications. ZnO is stable in air and environmentally safe. It has become an attractive wide band gap semiconductor since ultraviolet laser action was demonstrated

at room temperature [5]. Due to its transparent nature, it is of great importance to realize a transparent thin film transistor, which would be useful for driving an active matrix liquid crystal displays. By substituting the thin film transistors made of amorphous silicon or polycrystalline silicon currently used in active matrix liquid crystal displays by transparent ZnO thin film transistors [6]. Here ZnO-based metal–insulator–semiconductor junction has been fabricated using a low temperature Metal-Organic compound in a Plasma-Enhanced Chemical Vapour Deposition (MO-PECVD) system. High-performance, solution-processable semiconductors have drawn significant attention for use in low-cost, functional electronic applications. Metal oxide semiconductors are the most promising building blocks for high performance electronic devices because of their electrical properties and solution-processability [7]. However, the major impediment for metal oxide semiconductors is that the electrical properties applicable to electronic devices are activated by chemical/physical structural evolution at high temperatures, which critically limits the practical applications.

In this paper, I have studied the electrical and interfacial properties of metal oxide semiconductor structure fabricated on deposited SiO_2 films on ZnO/n-Si substrate by MO-PECVD system. The hysteresis voltage (ΔV_H), border trap density (Q_{bt}), interface state density (D_{it}) and fixed oxide charge density (Q_f /q) of the SiO_2/ZnO/Si films are found to 0.12 V, 3.9 x 10^{10} cm^{-2} , 8.37 × 10^{11} cm^{-2} eV^{-1} and 1.048 x 10^{11} cm^{-2} respectively.

2. Research Method

On the surface of Silicon wafers, along with possible contamination, there is a native oxide layer whose thickness is typically a couple of nanometers. This native oxide has to be completely removed in order that a good quality thin oxide film can be produced. It is also important that the substrate, its cleaning procedures and other processing stages are carefully selected.
Usually the wafers are first cleaned by using some chemical cleaning procedures [8]:

i. Clean ultrasonically in acetone (5 minutes),
ii. Rinse in deionized water (several times),
iii. Immerse in isopropyl alcohol (5 minutes),
iv. Immerse in H_2SO_4:H_2O_2 at 80 ^{0}C (10 minutes),
v. Rinse in deionized water (several times),
vi. Dip in 1% HF followed by rinsing in deionized water until the surface becomes hydrophobic.

Chemical cleaning procedures are used to remove all unwanted impurities from the surface. The quality of the resulting surface is usually good enough for the fabrication of conventional semiconductor devices. After chemical cleaning, it is possible to passivate the surface by HF treatment, for instance, which will prevent reactions with oxygen in the air or some other oxidizing species in the environment. The best way to remove the oxide is to do it in situ. This means it is done immediately before the beginning of oxidation and in the same processing equipment, reducing the risk of sample contamination. But for our case clean Silicon substrates were load into sputtering chamber followed by a dip in a dilute 1% HF solution.

Sputtering is the most extensively used technique for the deposition of Zinc Oxide [9]. This is closely followed by thermal evaporation [10], which can also be achieved using several different techniques. The choice of deposition technique is dictated by a number of factors such as quality and reproducibility of the ZnO film, homogeneity over a wide cross section, capacity, ease and cost of use as well as detrimental side effects and limitations specific to each technique. In addition, since the properties of ZnO depend strongly on the microstructure, stoichiometry and the nature of the impurities present, it is inevitable that each deposition technique with its associated controlling parameters should yield films with different characteristics.

A sputtering system consists of an evacuated chamber, a target (cathode) and a substrate (anode). The electric field inside a sputtering chamber accelerates electrons, which collide with Ar atoms producing Ar+ ions, and more electrons and characteristic purple/blue plasma. These charge particles are then accelerated by

Table 1. The typical growth parameters for deposition of ZnO on Si substrates

Base pressure	1.0×10^{-6} Torr.
Working pressure	1.0×10^{-2} Torr.
Target	Commercial ZnO (Pure.Tech. ~ 99.999 %)
Use gass	Argon
Substrate temperature	450 ^{0}C
Substrate	Si
RF power	100 W

the electric field, electrons towards the anode and Ar+ ions towards the cathode (ZnO target). In this study, ZnO (purity: 99.999%) films were deposited on Silicon substrate by 13.56 MHz rf magnetron sputtering

system. Table 1 shows the typical growth parameters for deposition of ZnO (110 nm) on Si substrates. A critical step for the MOS fabrication is to grow a high quality oxide film, which could be used for gate, mask and device isolation [11]. There is several techniques by which, high quality gate oxides usually deposit. Among them Plasma processing, now being routinely used in the device fabrication, because it is an alternative technique for low-temperature oxidation [12]. The most useful technique, which has replaced by the conventional atmospheric and low pressure CVD process, employs ionized plasma at a low pressure and very low sample temperature (40-400ºC). The method known as plasma enhanced chemical vapour deposition (PECVD) provides a low temperature chemical reaction due to the excitation of ions and neutrals by collisions with highly energetic electrons. This method of deposition satisfies many of the essential requirements, e.g., uniformity, low temperature processing, high throughput and better step coverage and low processing costs.

The deposition of SiO_2 was effected with decomposition of either tetraethylorthosilicate (TEOS) or a mixture of TEOS and oxygen. The pressure in this deposition was controlled by changing the TEOS bath temperature while keeping the throttle valve completely open. The pyrolysis of TEOS into SiO_2 can be representing by equation 1 [13]

$$SiO_4C_8H_{20} \rightarrow SiO_2 + 4C_2H_4 + 2H_2O \quad (1)$$

The reverse reaction is negligible, and the chemical reaction at the surface is assumed to be monomolecular decomposition, which is accompanied by adsorption/ decomposition process.

In our process flow, dielectric films were deposited on the ZnO/Si substrate using a microwave (1400 W, 2.45 GHz) plasma cavity discharge system. The base pressure of the process chamber was 1 mTorr. TEOS was kept in a bubbler whose temperature was set at 65ºC and the vapour was injected into the process chamber. Typically, a pressure of 1 Torr and a deposition time of 1 min were employed for film deposition (100 nm). No external heating of the substrate was made. For the electrical measurements, MOS test capacitors were fabricated on as-deposited layers with evaporated circular aluminum contacts (area: 1.96×10^{-3} cm^2) through a shadow mask.

3. Results and Analysis

The crystal quality and composition of the deposited films were analyzed with AFM, SEM, RBS and XPS. Semiconductor surface roughness is one of the most important parameters, which can adversely affect the performance and reliability of the devices [14]. Surface morphology of buffer layers is dependent on the processing conditions such as grading rate and growth temperature. Available optical techniques are often limited to 1D quantitative analysis of roughness. Atomic force microscopy has enabled the acquisition of highly accurate 3D topography over an extended scale with a high spatial resolution [15]. Typical measures of surface micro-roughness are the arithmetic mean deviation from a best fit plane surface of mean value (Z_{av}) and the square root of the sum of the squares of the deviation from the mean (Z_{rms}) of a specified area of the surface. These quantities are defined as follows [16]

$$Z_{av} = \frac{1}{N}\sum_{i=1}^{N}\left|z_i - \overline{Z}\right| \quad (2)$$

$$Z_{rms} = \left[\frac{1}{N}\sum_{i=1}^{N}\left|z_i - \overline{Z}\right|^2\right]^{1/2} \quad (3)$$

Here z_i is the height at the i-th sampling point (x, y), N is the number of data points and $\overline{Z}$ is the average z_i, i.e.

$$\overline{Z} = \frac{1}{N}\sum_{i=1}^{N} z_i \quad (4)$$

The scan was taken on an area of 25 μm^2. The statistical information of the topography of the ZnO films as

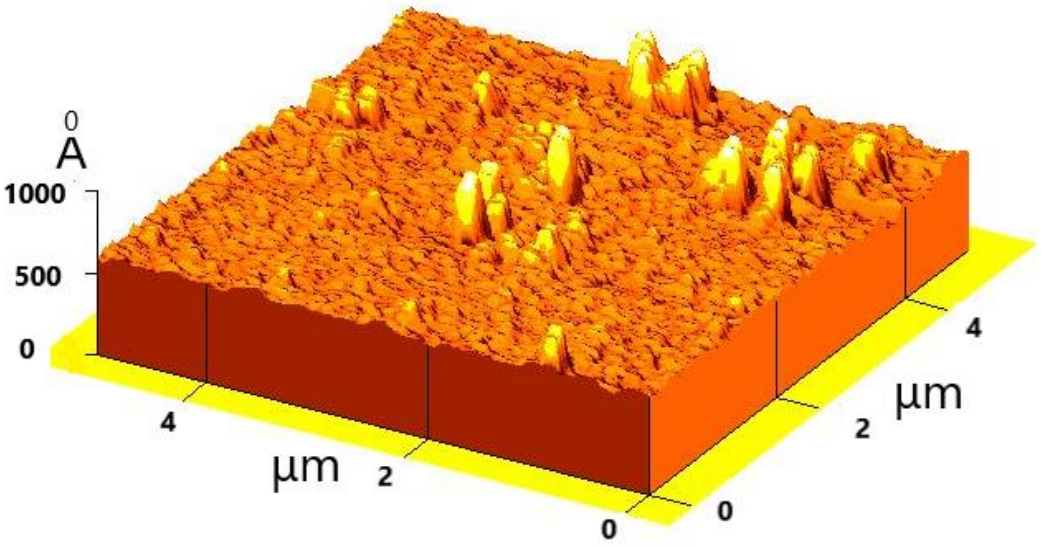

Figure 1. AFM topograph of of 3-D island for ZnO films grown on Si (100) at 450 °C.

observed from the height histogram from the AFM image of rms surface roughness (Z_{rms}) and average roughness Z_{av} 50.9 Å, 30.4 Å respectively from the figure 1 .

The surface morphology of the ZnO/Si films can be observed in figure 2. In figure, it is shown that structure is columnar.

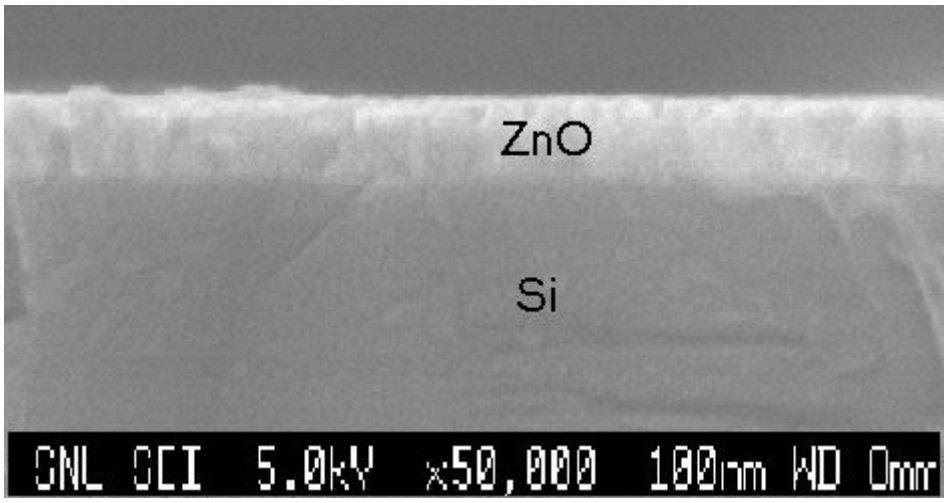

Figure 2. SEM view of the rf sputtered ZnO film deposited on Si.

Rutherford backscattering (RBS) analysis was carried out to estimate the composition and thickness of the films. The advantages of RBS are the following: (a) speed, (b) ability to perceive depth distribution of atomic species below the surface and (c) the quantitative nature of the results. RBS is used for depth profiling and layer removal of films by sputtering as used in SIMS or AES, is not involved. However, damage or defects are produced in the exposed films during RBS characterization [17].

2 MeV He^{+2} beams, attained through a charge exchange process with a stripper nitrogen gas, is normally used for the RBS and channeling measurements. The energy momentum of the beam is gained from a 90° analyzing magnet and the beam is directed to the scattering chamber through a switching magnet. The beam is collimated by a pair of collimators of diameter 1 mm separated by a distance of about half a meter. This is done to reduce the divergence of the beam, which is important for channeling measurements.

The surface barrier detector (SBD) (resolution 25 keV) can detect scattered particles over a scattering range of 0-170°. The solid angle subtended by the SBD is maintained around 2×10^{-3} steradian with the target. The beam current is in the range of 5-20 nA. The sample holder is a stainless steel vertical holder on which several

samples can be mounted. The energy of the beam and the scattering angle of the SBD can be changed without disturbing the vacuum system either in the chamber or in the accelerator. The sample position with respect to the beam can be varied vertically without breaking the vacuum. The data are collected by a MCDWIN (Version-1.0) multichannel analyzer attached to a data acquisition computer.

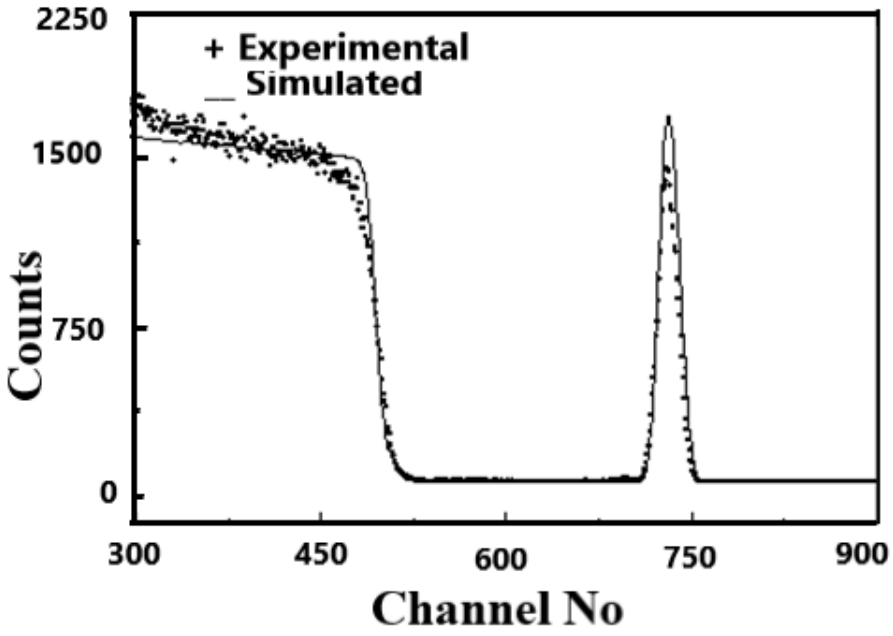

Figure 3. 2 MeV $^{4}He^{2+}$ Rutherford backscattering spectra of ZnO/Si sample: (+++) experimental and (---) simulated.

Different ion beam energies were used for the present study. Using bulk Si did the energy calibration and Au targets and the counting rate was kept 185-500 counts/sec for a particular set of study. In general, RBS is carried out at lower energies using He ions as the scattering cross-section for most of the elements are Rutherford type (Coulomb's law applies). In some cases, slightly higher energy was used for the present observations to estimate the relative composition accurately. However, the advantage of using higher energies lies in the fact that the overlap between the backscattered peaks is reduced and it is particularly important for multi-component films for which the stopping power decreases with increasing incident energy, resulting in narrower spectrum. The disadvantage is that the scattering cross-sections are more likely to become non-Rutherford and the value deviates by 4%. Figure 3 shows a typical RBS spectrum of ZnO/Si sample as described above. The scattered He^{+2} from the ZnO layer appears at higher energies (channel nos. 715-750) while those from the bulk Si substrate appear at lower energies (channel nos. 500-525).

Chemical state of a few nanometers surface layers is analyzed by X-ray photoelectron spectroscopy. XPS study was carried out using model ESCALAB MKII high vacuum system equipped with a concentric hemispherical analyzer (VG Microtech) with a residual gas pressure better than 1×10^{-8} Pa. Mg K_α X-rays ($h\nu$ = 1253.6 eV) radiation was used to excite the photoelectrons at an angle 0° to 30° between the analyzer axis and the sample normal. All spectra were taken at 300 K (room temperature). Figure 4 shows the broad energy XPS spectra of deposited SiO_2 films on ZnO/Si layers. High resolution recording of spectrum shows the XPS peak positions of Si 2p (104 eV) [18], Si 2s (149 eV), C 1s (284.5 eV), O 1s (532), and Zn 2p (1022 eV and 1045 eV) [19] for deposited SiO_2 on ZnO/Si, here Si 2p peak observed at 104 eV instead of 100 eV due to formation of SiO_2 on ZnO/Si layers is also shown in figure 5. Here the binding energies were corrected for sample with reference to the C 1s line around at 284.5 eV.

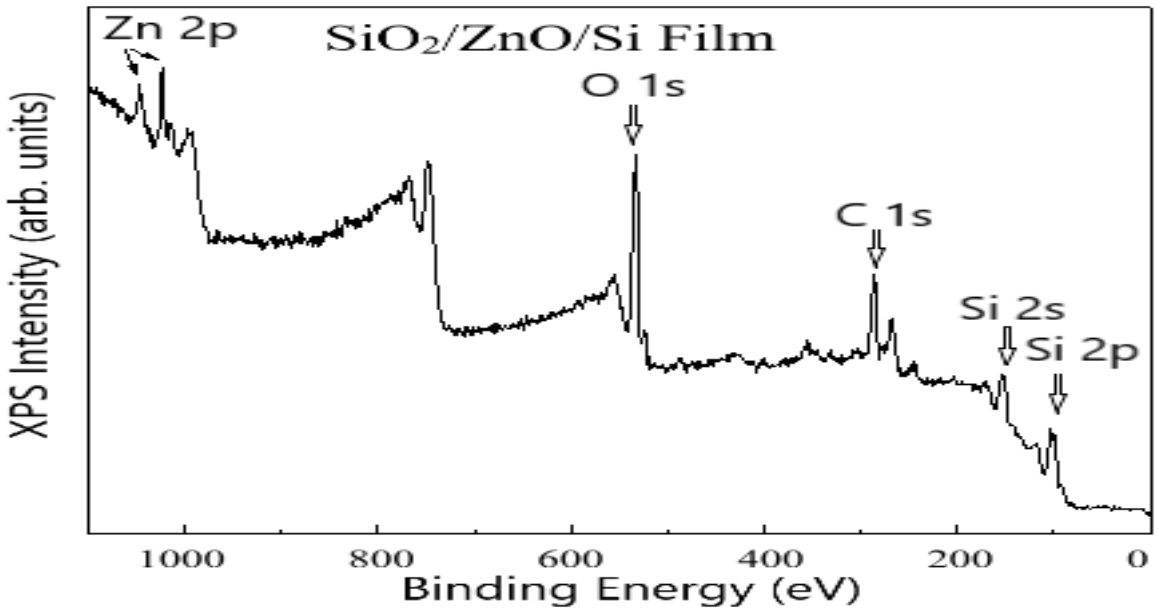

Figure 4. Broad scan XPS spectrum of SiO_2/ZnO/Si film shows characteristic peaks of Zn, O, C and Si.

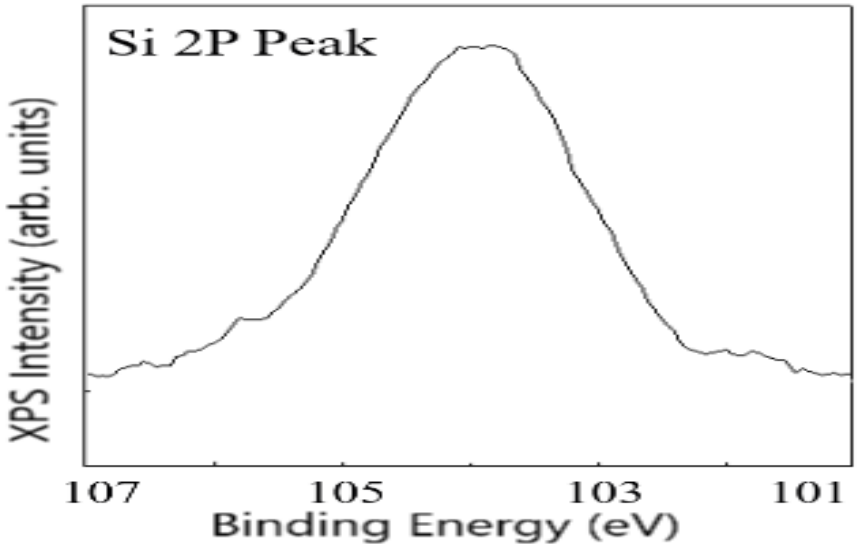

Figure 5. Typical Si 2p XPS spectra.

Figure 6 shows the high frequency (1 MHz) G-V characteristics of the Al/SiO_2/ZnO/Si capacitors and figure 7 shows the high frequency (1 MHz) C-V (HFCV) characteristics of Al/SiO_2/ZnO/n-Si MOS capacitors with a gate bias sweep from -5 to +5 V and back to -5 V at a rate of 0.1 Vs^{-1}. The gate voltage was swept from inversion to accumulation to get a forward high frequency C-V (HFCV) and from accumulation to inversion to get a reverse HFCV. These bidirectional HFCV curves exhibit a hysteresis. The hysteresis occurs due to the gate bias at which electrons fill the traps being different from the point at which the electrons leave the trap and/or due to the difference between the capture and emission times of the trap charges [20].

In an oxide, there are four important types of oxide and interface trap charges. The location of different types of charges trapped in a MOS structure is shown in figure 8 [21].

The first type of charge, the interface trapped charge (Q_{it}), is located at the oxide-semiconductor interface with energy states in the forbidden bandgap. Q_{it} is produced by excess Si (trivalent Si), excess oxygen, and impurities [22].

The second type of oxide charge, fixed oxide charge (Q_f), is the charge density remaining after the interface trap charge is annealed out. Q_f is generally a positive charge and located at the oxide-semiconductor interface.

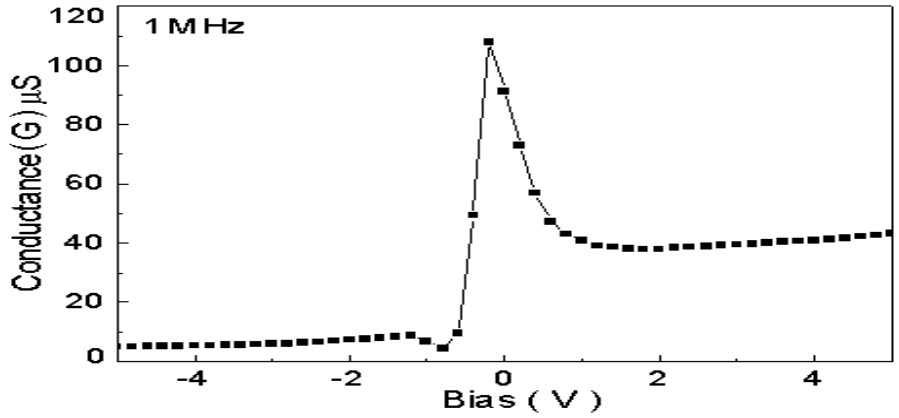

Figure 6. G-V characteristics of the Al/SiO_2/ZnO/Si capacitors.

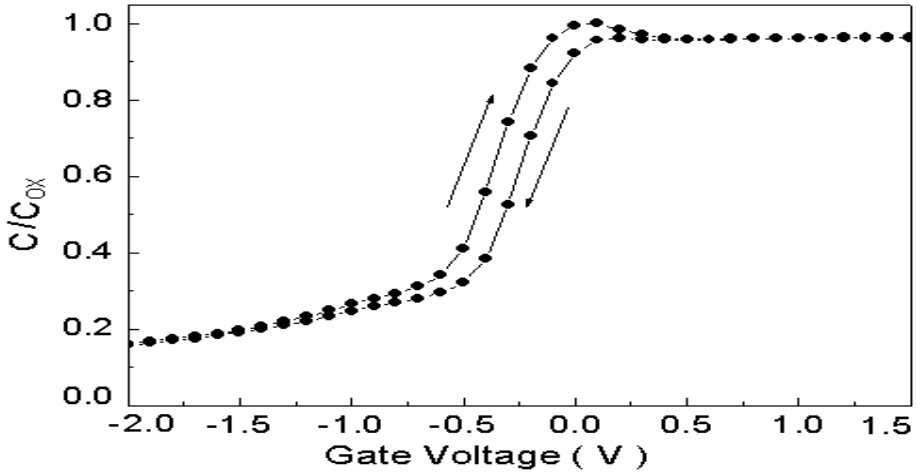

Figure 7. HFCV hysteresis of MOS capacitors on Al/SiO_2/ZnO/Si for voltage sweep from inversion to accumulation and back to inversion.

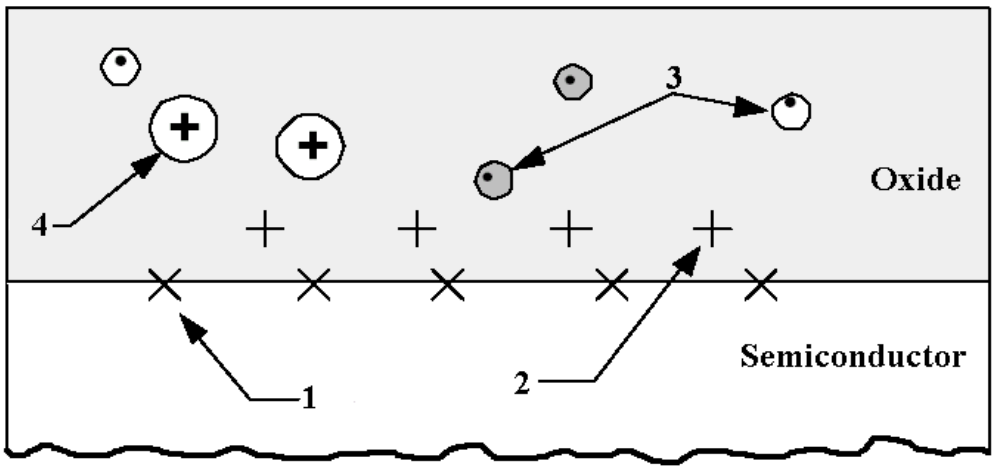

Figure 8. Location of trapped charges at different regions in the MOS structures.

The third type, oxide trapped charge (Q_{ot}), is usually located either at the metal-oxide interface or at the oxide-semiconductor interface. Q_{ot} is commonly produced by the injection of hot electrons or holes from avalanche plasma in a high field region in the Si, injection of carriers by photoemission or by exposure to ionizing radiation.

The fourth type, mobile ionic charge (Q_m), is caused by the presence of ionized alkaline metal atoms such as Na^+, Li^+, K^+, and possibly H^+. These types of charges are located either at the metal-oxide interface, where it originally enters the oxide layer, or at the oxide-semiconductor interface, where it has drifted under an applied field. Negative ions and heavy metals may contribute to this charge even though they are typically not mobile below 500 °C.

The oxide charge density is calculated from the difference between the experimentally determined and the ideal flatband voltages. The flatband voltage (V_{FB}) is related to the oxide charge and the work function difference between the metal and semiconductor (ϕ_{ms}). Oxide charges consist of the fixed oxide charge (Q_f), the oxide trapped charge (Q_{ot}) and the mobile ionic charge (Q_m). The contribution of Q_m is relatively small, as indicated by the absence of hysteresis effect in the experimental C-V characteristics and the low level of sodium contamination in the oxide during processing. The oxide-trapped charge (Q_{ot}) is generally assumed to be negligibly small at the low applied field used in C-V measurements. For simplicity, the presence of Q_f is assumed to be the only contributing factor for the flatband voltage shifts. The Q_f is then calculated using the relation

$$Q_f / q = \frac{C_{ox}}{A.q}\left(\phi_{ms} - \phi_F - V_{FB}\right) \qquad (5)$$

where C_{ox} is the oxide capacitance in accumulation, ϕ_F is the Fermi potential of semiconductor layers, V_{FB} is the flatband potential and A is the gate area of the capacitor.

The flatband voltage is determined using the flatband capacitance method. Silicon space charge capacitance C_{FBS} at the flatband condition is given by the relation

$$C_{FBS} = \varepsilon_{Si} / L_D \qquad (6)$$

where ε_{Si} is the permittivity of Si and L_D is the Debye length, expressed as

$$L_D = \left(\varepsilon_{Si} kT / q^2 p_0\right)^{1/2} \qquad (7)`$$

where p_0 is the equilibrium hole density in the semiconductor. The corresponding total high frequency flatband capacitance is given by

$$C_{FB} = C_{FBS} C_{ox} / \left(C_{FBS} + C_{ox}\right) \qquad (8)$$

The V_{FB} is then determined as the voltage at which the measured high-frequency capacitance is equal to the flatband capacitance.

The value of fixed oxide charge density (Q_f/q) is determined using the equation 5 where C_{ox}, the oxide capacitance in accumulation is 1.02×10^{-10} F, ϕ_{ms}, the work function difference between metal and semiconductor is -0.8 eV, ϕ_F, the Fermi potential of the heterolayers is -0.28 eV, V_{fb}, the flatband potential is -0.21 V, *A* the gate area of the capacitor is 1.96×10^{-3} cm^{-2}, The value of Q_f/q to be 1.048×10^{11} cm^{-2}.

The MOS capacitor is a useful tool for studying surface states at the semiconductor-insulator interface. This is particularly true for characterizing semiconductor devices in the microelectronics industry. Commonly used approximation techniques are difficult to interpret for interface state densities less than 10^{11} cm^{-2} eV^{-1}. Thus, a single frequency based Hill's [23] technique, which is an approximation method, and provides quantitative criteria on the quality of the interface, has been used in the present study. The data required are a single high frequency C-V measurement and a corresponding G-V measurement. This method is valid for low interface state density determination in a range from 7×10^9 to 8×10^{11} cm^{-2} eV^{-1}. The mathematical expression for calculating interface state density is given by

$$D_{it} = \left(2/q.A\right).\left(G_{\max}/\omega\right) \Big/ \left[\left(G_{\max}/\omega C_{ox}\right)^2 + \left(1 - C_m/C_{ox}\right)^2\right] \qquad (9)$$

where $G_{\max}$ is the maximum conductance in G-V plot with its corresponding capacitance (C_m), C_{ox} is the oxide capacitance, ω is the angular frequency and A is the area of the capacitor. The value of interface state density (D_{it}) was calculated from the G-V and C-V characteristics (shown in figure 6 and 7) using Hill's method by equation 9, is 8.37×10^{11} cm^{-2} eV^{-1}.

To improve the reliability of gate oxides, it is crucial to understand the nature of defects at and near the oxide-semiconductor interface. Interface traps are considered to be in rapid electrical communication with the underlying semiconductor, while oxide traps are not as codified in the Deal committee nomenclature. Trapping properties of MOS dielectric layers are most often evaluated via simple capacitance-voltage (C-V) and current–voltage (I-V) techniques. However, it has been shown that standard C-V and I-V techniques cannot easily be used to determine the total density of oxide traps in irradiated MOS devices [24]. Instead, they sense only the net density of trapped charges in the oxide. Schematically, we illustrate in figure 9 how this can be a problem. Assuming these are n-substrate capacitors and interface traps are charged negatively at flatband and are approximately charge neutral at midgap [25] and oxides (a) and (b) have equal flatband voltages. Still, oxide (a) is superior to oxide (b) because the extra oxide trap charge and interface traps in oxide (b) degrade device quality, performance and reliability. Thus, it is well known that one must obtain separate estimates of the densities of (net) oxide trap charge N_{ot} (generally taken to be proportional to the midgap voltage shift ΔV_{mg} and interface trap charge D_{it} generally taken to be proportional to C-V stretch out ΔV_{so} [26], and/or inferred from Terman, conductance, or related methods [27].

It is often assumed, at least tacitly, that the net oxide trap charge density N_{ot} can be equated to the density of trapped positive charge (generally holes) in the oxide, Q_h. However, this assumption is true only when the density of trapped negative charge Q_n in the oxide is small compared to Q_h. This is often presumed to be true for MOS radiation damage at modest dose levels [e.g., less than ~1 Mrad (SiO_2)] and for high-field stress at relatively low fluence (e.g., less than ~10^{-2} C/cm^2). When Q_n is not negligible, as in figure 9 (c) and (d), Q_n is less useful in assessing radiation or high field stress damage to an oxide. Comparing figures 9 (a) and (c) for example, one observes that there are twice as many trapped holes in figure 9 (c) and (d). However, half of the trapped holes in figure 9 (c) have their charge compensated by electrons near the semiconductor-oxide interface [27]. Figure 9 (d) is an even more extreme example. Here C-V data would reveal no net oxide charge, yet the total amount of trapped charge in the oxide is greater than in any other example. Oxides of figure 9 (c) and (d) are problems for most I-V and C-V methods, which sense either the net density of charged traps in the oxide, and/or changes in their charge states during the measurements [28]. They do not easily resolve dipolar defects consisting of compensating positive and negative charge, as shown in figure 9 (c) and (d), unless subsequent defect generation and/or annihilation studies are performed. For insulators that mostly trap one type of charge, this is not a major problem. Thermal oxides and oxynitrides can trap both electrons and holes when exposed to ionizing radiation or high-field stress [29].

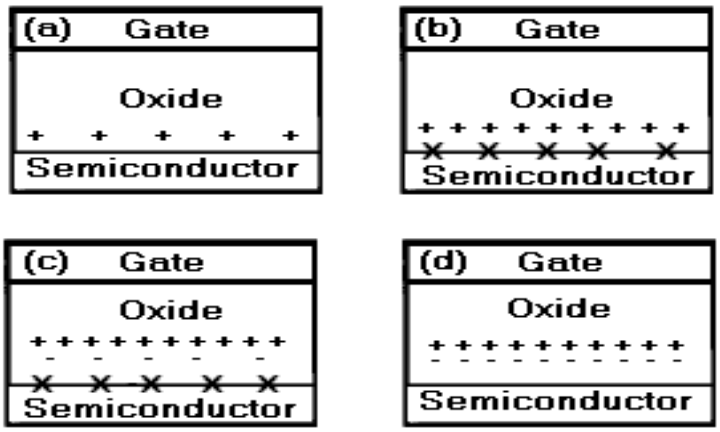

Figure 9. Schematic illustration of defect in MOS oxides. Shown are trapped holes in the oxide (+), compensating electrons in border traps (-), and interface traps (x).

However, the fact that the oxide traps close to the interface calls for the introduction of border traps (Q_{bt}) [30]. The border traps are charged and discharged through electrons tunneling from and to the substrate. The hysteresis in high frequency capacitance-voltage curve is commonly used to characterize the border traps [20]. The gate voltage is swept from inversion to accumulation to get a forward high frequency C-V (HFCV) and from accumulation to inversion to get a reverse HFCV. This bidirectional HFCV curves exhibit a hysteresis. The hysteresis occurs due to the gate bias at which electrons fill the traps is different from the point at which the electrons leave the trap and/or due to the difference between the capture and emission times of the border traps [30]. The border trap density is extracted from the hysteresis at the midgap capacitance (ΔV_H), assuming that the interface states do not contribute to the charge when the Fermi level is at the midgap.

$$Q_{bt} = \frac{C_{ox}\Delta V_H}{q.A} \qquad (10)$$

where C_{ox} is the gate oxide capacitance in accumulation region, q is the electronic charge, and A is the gate area. The hysteresis voltage (ΔV_H) is found to have a value of 0.12 V (in figure 7). The amount of hysteresis is a measure of border trap (Q_{bt}) and is given by equation 10, was found to be 3.9 $\times 10^{10}$ cm^{-2}.

4. Conclusion

In conclusion undoped ZnO (100 nm) thin films were deposited on Si (100) at 450 ^oC by rf magnetron sputtering. Metal-Organic compound in a plasma enhanced chemical vapor deposition of silicon dioxide from tetraethyl orthosilicate (TEOS) and oxygen plasma has been extensively investigated in this paper because of its wide-ranging applications in integrated circuit manufacturing and electronics technology as an insulator. The fixed oxide charge density, interface state density and border trap charges of $Al/SiO_2/ZnO/Si$ structures are found to be 1.048 $\times 10^{11}$ cm^{-2}, 8.37 $\times 10^{11}$ cm^{-2} eV^{-1} and 3.9 $\times 10^{10}$ cm^{-2} respectively. The hysteresis voltage (ΔV_H) of the said film is 0.12 V. It is shown that the low temperature microwave MO-PECVD techniques are useful for the deposition of good quality SiO_2 gate oxide directly on ZnO/n-Si for future electronic applications.

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